What it is claimed is:

1. A multi-layer capacitor device comprising:

a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces, the capacitor body including a plurality of first electrode plates and a plurality of second electrode plates, the first and second electrode plates being interleaved with each other in opposed and spaced apart relation;

a dielectric material located between each opposed set of the first and second electrode plates;

the first and second electrode plates each including a main electrode portion and a plurality of spaced apart lead structures extending therefrom, respective lead structures of the first electrodes plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement; and

a plurality of electrical terminals located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body; wherein

each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is

disposed opposite to another of the second polarity terminals across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

2. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 1.3 or less.

3. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 0.4 or greater.

4. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

5. The multi-layer capacitor according to claim 1, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

6. The multi-layer capacitor according to claim 1, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

7. The multi-layer capacitor according to claim 1, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

8. The multi-layer capacitor according to claim 1, wherein the capacitor body has a substantially rectangular shape.

9. The multi-layer capacitor according to claim 1, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

10. The multi-layer capacitor according to claim 1, wherein at least one of the first polarity terminals is provided at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

11. The multi-layer capacitor device according to claim 1, wherein the first polarity terminals are disposed opposite to each other across a width of the ~~substantially rectangular~~ capacitor body.

12. The multi-layer capacitor device according to claim 1, wherein the second polarity terminals are disposed opposite to each other across a width of the capacitor body.

13. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals only across a width of the capacitor body.

14. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals only across a width of the capacitor body.

15. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals and the corresponding another of the first polarity terminals are located at a common position along a length of the capacitor body.

16. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals and the corresponding another of the second polarity terminals are located at a common position along a length of the capacitor body.

17. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

18. The multi-layer capacitor device according to claim 1, wherein the electrical terminals extend to portions of the top and bottom surfaces.

19. The multi-layer capacitor device according to claim 1, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

20. The multi-layer capacitor device according to claim 1, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

21. The multi-layer capacitor device according to claim 1, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

22. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

23. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

24. A multi-layer capacitor device according to claim 1, wherein the multi-layer capacitor device is arranged to define a decoupling capacitor for a multiprocessing unit.

25. A high frequency circuit comprising at least one multi-layer capacitor device according to claim 1.

26. The high frequency circuit according to claim 25, wherein the at least one multi-layer capacitor device is arranged to define one of a bypass capacitor and a decoupling capacitor.

27. A wiring substrate comprising at least one multi-layer capacitor device according to claim 1 mounted thereon.

28. A multi-layer capacitor device comprising:

a capacitor body including a pair of opposed side surfaces having continuously smooth surfaces and a pair of opposed end surfaces disposed between the pair of opposed side surfaces;

at least four electrical terminals disposed on each of the opposed side surfaces;

the capacitor body also including at least one first electrode plate having a ~~generally~~ substantially rectangular first main electrode portion with a plurality of first lead structures extending therefrom and at least one second electrode plate situated in opposed and spaced apart relation to the first electrode plate, the second electrode plate having a ~~generally~~ substantially rectangular second main electrode portion with a plurality of second lead structures extending therefrom, respective ones of the first lead structures being located adjacent respective ones of the second lead structures in an interdigitated arrangement and extending to respective ones of the electrical terminals;

dielectric material disposed between each opposing set of first and second electrode plates; wherein

each of the lead terminals of the at least one first electrode plate being disposed opposite to another of the lead terminals of the at least one first electrode plate across the capacitor body and each of the lead terminals of the at least one second electrode plate being disposed opposite to another of the lead terminals of the at least one second electrode plate across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

29. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to about 1.3 or less.

30. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to about 0.4 or greater.

31. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

32. The multi-layer capacitor device according to claim 28, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

33. The multi-layer capacitor device according to claim 28, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

34. The multi-layer capacitor device according to claim 28, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

35. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a width of the substantially rectangular capacitor body.

36. A multi-layer capacitor device according to claim 28, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the substantially rectangular capacitor body.

37. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a width of the ~~substantially rectangular~~ capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the ~~substantially rectangular~~ capacitor body.

38. The multi-layer capacitor device according to claim 28, wherein the capacitor body has a substantially rectangular shape.

39. The multi-layer capacitor device according to claim 28, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

40. The multi-layer capacitor device according to claim 28, wherein at least one of the first polarity terminals is provided at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

41. The multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

42. The multi-layer capacitor device according to claim 28, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

43. The multi-layer capacitor device according to claim 28, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

44. The multi-layer capacitor device according to claim 28, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

45. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

46. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

47. A multi-layer capacitor device according to claim 28, wherein the multi-layer capacitor device is arranged to define a decoupling capacitor for a multiprocessing unit.

48. A high frequency circuit comprising at least one multi-layer capacitor device according to claim 28.

49. The high frequency circuit according to claim 48, wherein the at least one multi-layer capacitor device is arranged to define one of a bypass capacitor and a decoupling capacitor.

50. A wiring substrate comprising at least one multi-layer capacitor according to claim 28 mounted thereon.

51. A monolithic capacitor comprising:

a capacitor body having two opposed main surfaces and four side surfaces connected between the two main surfaces, said capacitor body including a plurality of dielectric layers extending in the direction in which the two opposed main surfaces extend, and at least one pair of first and second internal electrodes opposed to each other through one of the dielectric layers so as to define a capacitor unit, said capacitor body further including at least two first lead electrodes extending from one of the first internal electrodes to at least two positions on at least one of the side surfaces, and at least one second lead electrode extending from the second internal electrode to a position located between the positions to which the first lead electrodes extend;

first and second external terminal electrodes provided on the side surfaces onto which the first and second lead electrodes extend, and electrically connected to the first and second lead electrodes, respectively; wherein

the ratio L/W of the length L to the width W of at least one of the first and second lead electrodes is within the range of about 0.4 to about 3.0.

52. A monolithic capacitor according to Claim 51, wherein the ratio L/W is in the range of about 0.4 to about 1.3.

53. A monolithic capacitor according to Claim 51, wherein the first and second lead electrodes extend onto at least two of the side surfaces opposed to each other, respectively.

54. A monolithic capacitor according to Claim 51, wherein at least one of the first and second lead electrodes extend onto the respective four side surfaces.

55. A monolithic capacitor according to Claim 51, wherein the first lead electrodes and the second lead electrodes are alternately arranged as viewed in the peripheral directions of the main surfaces.

56. A monolithic capacitor according to Claim 51, wherein the monolithic capacitor is arranged to define a decoupling capacitor connected to a power supply circuit of an ~~MPU~~ microprocessing unit chip provided in a microprocessing unit.

57. A wiring substrate including the monolithic capacitor according to Claim 51 mounted thereon.

58. A wiring substrate including the monolithic capacitor according to Claim 57, further comprising an ~~MPU~~ microprocessing unit chip of a microprocessing unit mounted on the wiring substrate.

59. A decoupling circuit including the monolithic capacitor according to Claim 51.

60. A high frequency circuit including the monolithic capacitor according to Claim 51.